REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

I. Disposition of Claims

Claims 1-33 are currently pending in the present application.

II. Double Patenting Rejection(s)

Claims 1-33 of the present application were rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-33 of U.S. Patent No. 6,819,192 in view of Heydari et al. However, this rejection is improper because U.S. Patent No. 6,819,192 is not prior art to the present application. Both the present application and U.S. Patent No. 6,819,192 were filed on February 14, 2002. In order to sustain an obviousness-type double patenting rejection, each invalidating reference must be prior art. This is not the case here as U.S. Patent No. 6,819,192 is not prior art to the present application. Accordingly, this rejection is improper and withdrawal of same is respectfully requested.

III. Rejection(s) Under 35 U.S.C § 103

Claims 1, 4, 5, 7, 9-12, 15-16, 18, 20-23, 26, 27, 29, and 31-33

Claims 1, 4, 5, 7, 9-12, 15-16, 18, 20-23, 26, 27, 29, and 31-33 of the present application were rejected under 35 U.S.C. § 103(a) as being unpatentable over Heydari et

al. For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a simulating technique for optimizing decoupling capacitance in a phase locked loop. As recited in independent claims 1, 12, and 23 of the present application, the simulation technique requires (i) inputting a representative power supply waveform having noise to a simulation of the phase locked loop, (ii) estimating jitter of the phase locked loop, (iii) adjusting an amount of decoupling capacitance, and (iv) repeating the inputting, estimating, and adjusting until the jitter falls below a selected amount.

Heydari fails to disclose the above recited limitations of the claimed invention. For example, the Examiner relies on Figure 2 of Heydari of disclosing the claimed limitation of adjusting an amount of decoupling capacitance. However, Heydari clearly states that Figure 2 shows the supply noise without a decoupling capacitor (Figure 2a) and with a decoupling capacitor (Figure 2b). *See* Heydari, page 444 (top-left paragraph). Heydari is completely silent as to adjusting and optimizing an amount of decoupling capacitance as required by the claimed invention. Heydari simply shows the effect of decoupling capacitance on supply noise, but is not at all concerned with optimizing an amount of decoupling capacitance. Thus, Heydari clearly fails to disclose each and every limitation of independent claims 1, 12, and 23 of the present application.

Moreover, Heydari discloses a mathematical model for estimating the amount of jitter given particular input to the model. *See, e.g.*, Heydari, page 446 (section VII). That mathematical model is tested by taking the inputs to the model and applying them to a phase locked loop and comparing the results to the results predicted by the model. *See id.* However, this is entirely distinct from inputting a representative power supply waveform

to a simulation of a phase locked loop, estimating jitter, adjusting a decoupling capacitance, and repeating these simulation steps until a desired decoupling capacitance is achieved. While Heydari endeavors to create a mathematical model for a phase locked loop, the claimed invention is directed to performing simulation to achieve a desired level of decoupling capacitance. Accordingly, Heydari clearly fails to disclose, or otherwise teach, each and every limitation of independent claims 1, 12, and 21 of the present application.

In view of the above, Heydari fails to show or suggest the present invention as recited in independent claims 1, 12, and 23 of the present application. Thus, independent claims 1, 12, and 23 are patentable over Heydari. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this § 103 rejection is respectfully requested.

Claims 2, 3, 6, 8, 13, 14, 17, 19, 24, 25, 28, and 30

Claims 2, 3, 6, 8, 13, 14, 17, 19, 24, 25, 28, and 30 of the present application were rejected under 35 U.S.C. § 103(a) as being unpatentable over Heydari in view of Applicant's Admitted Prior Art (AAPA). For the reasons set forth below, this rejection is respectfully traversed.

As discussed above, Heydari fails to disclose each and every limitation of independent claims 1, 12, and 23 of the present application. Like Heydari, AAPA also fails to disclose each and every limitation of the claimed invention or supply that which Heydari lacks. AAPA is completely silent as to a step for adjusting decoupling capacitance during a simulation of a phase locked loop. Accordingly, AAPA fails to

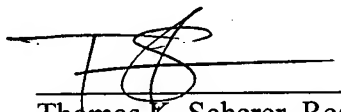
disclose at least those limitations of independent claims 1, 12, and 23 not disclosed in Heydari.

In view of the above, Heydari and AAPA, whether considered separately or in combination, fail to show or suggest the present invention as recited in independent claims 1, 12, and 23 of the present application. Thus, independent claims 1, 12, and 23 are patentable over Heydari and AAPA. Dependent claims 2, 3, 6, 8, 13, 14, 17, 19, 24, 25, 28, and 30 are allowable for at least the same reasons. Accordingly, withdrawal of this § 103 rejection is respectfully requested.

IV. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.171001; P7189).

Respectfully submitted,



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